# PATENT ABSTRACTS OF JAPAN

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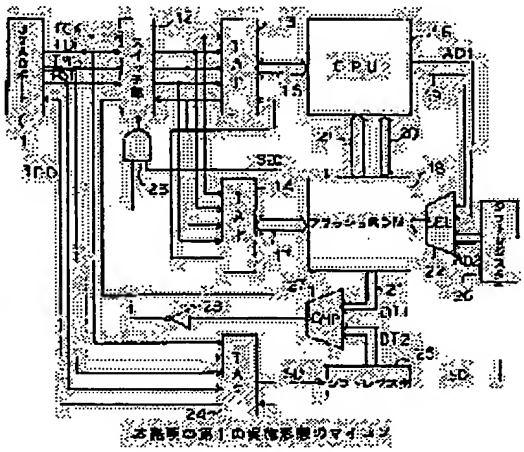
## (54) MICROCOMPUTER

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a microcomputer which can use a JTAG port by specific operation even after a security bit is set.

SOLUTION: When an address AD2 and data DT2 are inputted from the JTAG port 11, those address AD2 and data DT2 are held in shift registers 26 and 25 respectively through TAP 24. The address AD2 is given to a flash ROM and the data DT1 in the address specified by the address AD2 are read out and outputted to a comparator 27. The data DT2 held in the shift register 25 are also outputted to the comparator 27. When the data DT1 and DT2 match each other, the output of the comparator 27 goes up to 'H' and the output of an AND 23 becomes 'L' irrelevantly to a security signal SEQ. Consequently, a switch part 12 turns on and the JTAG port 11 is connected to TAPs 13 and 14 through the switch part 12.

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CLAIMS

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[Claim(s)]
[Claim 1] The storage which memorizes the program and data for control processing, and the central processing unit which performs predetermined control processing according to said program, In the microcomputer which has the trial port which outputs and inputs a stimulus, and the switch which turns on/controls [ off ] said trial port and store and/or a central processing unit, and between according to the security bit set as the register of a non-volatile The microcomputer characterized by establishing the security discharge means which makes said switch an ON state when the data inputted into said trial port are compared with the data memorized by said store and both are in agreement.
[Claim 2] The address register which said security discharge means holds the address information inputted from said trial port, and specifies the storage region of said store, The data register holding the data information inputted from said trial port, The comparator in comparison with the data held at said data register in the data by which reading appearance was carried out from said store according to said address information, The microcomputer according to claim 1 characterized by having the logic gate which sets said switch as an ON state irrespective of the condition of said security bit when the comparison result of said comparator is coincidence.
[Claim 3] The address counter which said security discharge means counts the timing information by which a sequential input is carried out from said trial port, and specifies the storage region of said storage, The data register holding the data information inputted from said trial port corresponding to said timing information, The comparator in comparison with the data held at said data register in the data by which reading appearance was carried out from said store according to assignment of said address counter, The count counter of coincidence which outputs a discharge signal when the count whose comparison result of said comparator corresponded is counted and the result reaches a predetermined value, The microcomputer according to claim 1 characterized by having the logic gate which sets said switch as an ON state irrespective of the condition of said security bit when said discharge signal is given.
[Claim 4] The microcomputer according to claim 3 characterized by preparing the address register which holds the address information inputted from said trial port, and sets up the initial value of said address counter.
[Claim 5] The storage which memorizes the program and data for control processing, and the central processing unit which performs predetermined control processing according to said program, The trial port which outputs and inputs a stimulus, and the switch which turns on/controls [ off ] said trial port and said central processing unit, and between, The microcomputer characterized by having the security discharge means which makes said switch an ON state when the data inputted into said trial port are compared with the data memorized by said store and both are in agreement.

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## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is equipped with the trial port for debugging, and relates to the microcomputer (henceforth a "microcomputer") which has a security bit for forbidding access by this trial port after debugging termination.
[0002]
[Description of the Prior Art] Drawing 2 is the block diagram of the microcomputer which has the conventional security bit. This microcomputer has the JTAG (Joint Test Action Group) port 11 which is an interface for connecting debugging equipment etc. at the time of debugging. The JTAG port 11 outputs and inputs the signal and serial data of clock signal TCK for a trial, input data TDI, the mode selection signal TMS, reset-signal TRST, output data TDO, etc.
[0003] The JTAG port 11 is connected to TAP (Test Access Port) 13 and 14 through the switch section 12. When it will be in an ON state and between the JTAG port 11 and TAP 13 and 14 is connected, when the security signal SEQ later mentioned for a control terminal is not given, and the security signal SEQ is given, the switch section 12 will be in an OFF state, and separates between the JTAG port 11 and TAP 13 and 14.
[0004] TAP13 is connected to a central processing unit (henceforth "CPU") 16 through the control line 15, and TAP14 is connected to the flash ROM (rewritable nonvolatile memory) 18 through the control line 17. TAP13 outputs the condition of this CPU16 etc. to a debugging equipment side while it decodes the stimulus given through the JTAG port 11 from debugging equipment at the time of debugging and controls CPU16. Moreover, TAP14 decodes a stimulus and write the data of a flash ROM 18. [ reading and ]
[0005] CPU16 and the flash ROM 18 are connected with the address bus 19, the control bus 20, and the data bus 21. The flash ROM 18 has the register with which the rewritable non-volatile called a security bit became independent, and when this register is set, said security signal SEQ is given to the control terminal of the switch section 12.
[0006] With such a microcomputer, when data are not written in a flash ROM 18, the security bit is in the reset condition and the security signal SEQ is not outputted. Therefore, the JTAG port 11 is connected to TAP 13 and 14 through the switch section 12.
[0007] While connecting debugging equipment to the JTAG port 11 and writing data and a program in a flash ROM 18 in this condition, a check of operation, program debugging, etc. of CPU16 are performed. And when debugging is completed, a security bit is set with the command from debugging equipment.
[0008] If a security bit is set, the security signal SEQ will be outputted from a flash ROM 18, and the switch section 12 will be in an OFF state. The JTAG port 11 is separated from TAP 13 and 14, and it becomes impossible thereby, to access CPU16 and a flash ROM 18 through this JTAG port 11 from the exterior. Thus, security, such as CPU16 of a microcomputer and data in a flash ROM 18, is protected.
[0009]
[Problem(s) to be Solved by the Invention] However, the following technical problems occurred with the

conventional microcomputer. For example, after writing the completed program in a flash ROM 18 and shipping as a product, the bug of a program may need to be discovered or it may be necessary to change fixed data by specification modification. In such a case, since the JTAG port 11 cannot be used, this microcomputer must be discarded. Moreover, it may be necessary to exchange the whole equipment which incorporated this microcomputer depending on the case.

[0010] Also after this invention solves the technical problem which said conventional technique had and sets a security bit, it offers the microcomputer which can use the JTAG port 11 by specific actuation.

[0011]

[Means for Solving the Problem] In order to solve said technical problem, the 1st invention of this inventions The storage which memorizes the program and data for control processing, and CPU which performs predetermined control processing according to said program, In the microcomputer which has the trial port which outputs and inputs a stimulus, and the switch which turns on/controls [ off ] said trial port and store and/or CPU, and between according to the security bit set as the register of a non-volatile The data inputted into said trial port are compared with the data memorized by said store, and when both are in agreement, the security discharge means which makes said switch an ON state is established.

[0012] The address register which the 2nd invention holds the address information into which the security discharge means in the 1st invention is inputted from a trial port, and specifies the storage region of a store, The data register holding the data information inputted from said trial port, The comparator in comparison with the data held at said data register in the data by which reading appearance was carried out from said store according to said address information, When the comparison result of said comparator is coincidence, said switch consists of logic gates set as an ON state irrespective of the condition of said security bit.

[0013] The address counter which the 3rd invention counts the timing information by which a sequential input is carried out from a trial port in the security discharge means in the 1st invention, and specifies the storage region of storage, The data register holding the data information inputted from said trial port corresponding to said timing information, The comparator in comparison with the data held at said data register in the data by which reading appearance was carried out from said store according to assignment of said address counter, The count counter of coincidence which outputs a discharge signal when the count whose comparison result of said comparator corresponded is counted and the result reaches a predetermined value, When said discharge signal is given, said switch consists of logic gates set as an ON state irrespective of the condition of said security bit.

[0014] The 4th invention has prepared the address register which holds the address information inputted from a trial port on the microcomputer of the 3rd invention, and sets the initial value of an address counter as it.

[0015] According to the 1st – the 4th invention, since the microcomputer was constituted as mentioned above, the following operations are performed.

[0016] An input of the data information memorized from the trial port to the address information and the address of a store holds such address information and data information at an address register and a data register, respectively. The storage region of a store is specified by the address information held at the address register, and reading appearance of the data memorized from this store is carried out. The data by which reading appearance was carried out from the store are given to a comparator, and are compared with the data held at the data register. The comparison result of a comparator is given to a logic gate, and when this comparison result is coincidence, a switch is set as an ON state irrespective of the condition of a security bit.

[0017] The storage with which the 5th invention memorizes the program and data for control processing in a microcomputer, CPU which performs predetermined control processing according to said program, and the trial port which performs I/O of a stimulus, When the switch which turns on/controls [ off ] said

trial port and said CPU, and between, and the data inputted into said trial port are compared with the data memorized by said store and both are in agreement, it has the security discharge means which makes said switch an ON state.

[0018] According to the 5th invention, the following operations are performed. When data are inputted into a trial port, this data is given to a security discharge means and compared with the data memorized by the store. And if both are in agreement, a switch is made into an ON state by the security discharge means, between a trial port and CPUs will be connected and I/O of the stimulus over this CPU will be attained.

[0019]

[Embodiment of the Invention] (1st operation gestalt) Drawing 1 is the block diagram of the microcomputer in which the 1st operation gestalt of this invention is shown, and the common sign is given to the element in drawing 2 R> 2, and the common element. This microcomputer has the JTAG port 11 which is an interface for connecting debugging equipment etc. at the time of debugging. The JTAG port 11 outputs and inputs the signal and serial data of clock signal TCK for a trial, input data TDI, the mode selection signal TMS, reset-signal TRST, output data TDO, etc.

[0020] The JTAG port 11 is connected to TAP 13 and 14 through the switch section 12. When for example, a control terminal is level "L", the switch section 12 will be in an ON state, will connect between the JTAG port 11 and TAP 13 and 14, will be in an OFF state at the time of level"H", and separates between the JTAG port 11 and TAP 13 and 14.

[0021] TAP13 is connected to CPU16 through the control line 15, and TAP14 is connected to the flash ROM 18 through the control line 17. TAP13 outputs the condition of this CPU16 etc. to a debugging equipment side while it decodes the stimulus given through the JTAG port 11 from debugging equipment at the time of debugging and controls CPU16. Moreover, TAP14 decodes a stimulus at the time of debugging, and write the data of a flash ROM 18. [ reading and ]

[0022] CPU16 and a flash ROM 18 are connected with a control bus 20 and a data bus 21, and address signal AD1 outputted from this CPU16 is given to a flash ROM 18 through a selector (SEL) 22 from an address bus 19. Moreover, the flash ROM 18 has the register with which the rewritable non-volatile called a security bit became independent, and the output signal of this register is given to the control terminal of the switch section 12 through AND (AND gate)23.

[0023] Furthermore, this microcomputer has TAP24 connected without JTAG minding [ 11 ] a switch. TAP24 outputs serial data SD according to the clock signal TCK and input data TDI which were given from the JTAG port 11. Moreover, TAP24 has the function to relay the output data TDO between the switch section 12 and the JTAG port 11.

[0024] The serial data SD outputted from TAP24 is inputted into the shift register 25 for data, and the serial output side of this shift register 25 is further given to the shift register 26 for the addresses. Shift registers 25 and 26 carry out a sequential shift, hold the data inputted into the serial, and output them as parallel data.

[0025] The juxtaposition output side of shift registers 25 and 26 is connected to the 2nd input side of a comparator (CMP) 27 and a selector 22, respectively. The 1st input side of a comparator 27 is connected to the data bus 21. A comparator 27 compares the data given to the 1st and 2nd input sides, when in agreement, the output signal of "H" is outputted, and the output side of this comparator 27 is connected to the 2nd input side of AND23 through the inverter 28.

[0026] Next, actuation is explained. In the microcomputer of drawing 1 , actuation when the security bit of a flash ROM 18 is not set is the same as that of the microcomputer of drawing 2 . That is, the security signal SEQ outputted from a flash ROM 18 is "L", the switch section 12 will be in an ON state, and the JTAG port 11 is connected to TAP 13 and 14 through this switch section 12. Moreover, by the control signal which a selector 22 does not illustrate, the 1st input side is chosen and address signal AD1 of CPU16 is given to a flash ROM 18.

[0027] While connecting debugging equipment to the JTAG port 11 and writing data and a program in a flash ROM 18 in this condition, a check of operation, program debugging, etc. of CPU16 are performed. And when debugging is completed, a security bit is set with the command from debugging equipment.
[0028] If a security bit is set, the security signal SEQ outputted from a flash ROM 18 will serve as "H". Moreover, since the output signal of a comparator 27 is usually "L", the output signal of AND23 will serve as "H", and the switch section 12 will be in an OFF state. By this, the JTAG port 11 is separated from TAP 13 and 14, access to CPU16 or a flash ROM 18 is forbidden through this JTAG port 11 from the exterior, and the security of a microcomputer is protected. On the other hand, CPU16 is connected with a flash ROM 18 through an address bus 19, a control bus 20, and a data bus 21, and predetermined control processing is performed based on the program written in this flash ROM 18.
[0029] Here, in order to correct debugging for analyzing malfunction of a microcomputer, the program for example, in a flash ROM 18, etc., the actuation in the case of canceling a security bit is explained.
[0030] First, debugging equipment is connected to the JTAG port 11, and a command with which a selector 22 chooses the 2nd input side is inputted. Thereby, an address bus 19 is separated and the juxtaposition output side of a shift register 26 is connected to the address terminal of a flash ROM 18 through a selector 22.
[0031] Next, since the content of storage of a flash ROM 18 is known for those who debug, it gives the data DT 2 corresponding to the address AD 2 and the address AD 2 of arbitration continuously to the JTAG port 11 from debugging equipment. The address AD 2 and data DT 2 are sent to TAP24 one by one, and are outputted to shift registers 25 and 26 as serial data SD from this TAP24. With shift registers 25 and 26, serial data SD carries out a sequential shift, and is held. Thereby, the address AD 2 and data DT 2 are held at shift registers 26 and 25, respectively.
[0032] The address AD 2 held at the shift register 26 is given to the address terminal of a flash ROM 18 through a selector 22, and the content DT 1 of the address AD 2 of this flash ROM 18, i.e., data, is outputted to a data bus 21. Moreover, the data DT 2 held at the shift register 25 are given to the 2nd input side of a comparator 27. And in a comparator 27, the data DT 1 by which reading appearance was carried out from the flash ROM 18 are compared with the data DT 2 given from debugging equipment. Since data DT1 and DT2 are naturally equal, the output signal of a comparator 27 will serve as "H", the output signal of AND23 will be set to "L", and the switch section 12 will be in an ON state.
[0033] Thereby, it can connect with TAP 13 and 14 and the JTAG port 11 can access now CPU16 and a flash ROM 18 from debugging equipment. Here, if the security bit of a flash ROM 18 is reset from debugging equipment, the security signal SEQ will be set to "L" and a microcomputer will be returned to the condition which can be debugged.
[0034] As mentioned above, it has the comparator 27 which compares whether the shift registers 26 and 25 which shift and hold the address AD 2 and Data DT 2 which were given to the JTAG port 11 through TAP24 by which direct continuation is carried out, and this TAP24, the data DT 1 which accessed the flash ROM 18 and read it according to the content of maintenance of this shift register 25, and the data DT 2 of the microcomputer of this 1st operation gestalt of a shift register 26 correspond. There is an advantage that only those who know the stored data of a flash ROM 18 can cancel a security bit by this.
[0035] (2nd operation gestalt) Drawing 3 is the block diagram of the microcomputer in which the 2nd operation gestalt of this invention is shown, and the common sign is given to the element in drawing 1, and the common element.
[0036] This microcomputer was replaced with the shift register 26 in drawing 1, and while forming the counter 29 which counts clock signal CK given from TAP24, the counter 30 which counts the comparison result of a comparator 27 is formed. The output signal of a counter 29 is given to a flash ROM 18 through a selector 22 as the address AD 2. Moreover, when counted value exceeds constant value, the overflow signal OVF is made into "H", and is outputted, and, as for a counter 30, this overflow

signal OVF is given to the 2nd input side of AND23 through an inverter 28. Other configurations are the same as that of drawing 1 .

[0037] In such a microcomputer, discharge of the once set security bit is performed as follows.

[0038] First, debugging equipment is connected to the JTAG port 11, and a command with which a selector 22 chooses the 2nd input side is inputted. Thereby, an address bus 19 is separated and the output side of a counter 29 is connected to the address terminal of a flash ROM 18 through a selector 22. Moreover, the command which clears the value of counters 29 and 30 to 0 is inputted.

[0039] Next, the 0th data DT 2 of a flash ROM 18 are given to the JTAG port 11 from debugging equipment. From the JTAG port 11, through TAP24, data DT 2 are given to a shift register 25, and are held. The data DT 2 held at the shift register 25 are given to the 2nd input side of a comparator 27. On the other hand, since the value of a counter 29 is 0, reading appearance of the 0th content is carried out from a flash ROM 18, and it is given to the 1st input side of a comparator 27 as data DT 1. Since data DT1 and DT2 are naturally equal, the output signal of a comparator 27 serves as "H", and the value of a counter 30 increases and is set to 1.

[0040] Then, while giving the 1st data DT 2 of a flash ROM 18 to the JTAG port 11 from debugging equipment, only 1 makes the value of a counter 29 increase by clock signal CK. Thereby, the data DT 2 given from debugging equipment are compared with the data DT 1 by which reading appearance was carried out from the 1st street of a flash ROM 18. Since both are naturally equal, the value of a counter 30 increases and is set to 2.

[0041] If similarly the sequential input of the data of all the addresses of a flash ROM 18 is carried out and all data are in agreement, the overflow signal OVF will be outputted from a counter 30. Thereby, the output signal of AND23 will be set to "L", and the switch section 12 will be in an ON state. Subsequent actuation is the same as that of the 1st operation gestalt.

[0042] As mentioned above, the microcomputer of this 2nd operation gestalt has the counter 30 which compares the shift register 25 holding the data DT 2 given to the JTAG port 11 through TAP24 by which direct continuation is carried out, and this TAP24, the counter 29 which carries out sequential count-up of address signal AD2, and is given to a flash ROM 18, and the data DT 1 by which reading appearance was carried out from this flash ROM 18 with the data DT 2 given from debugging equipment, and counts the count of coincidence. Only those who know all the stored data of a flash ROM 18 are able to cancel a security bit by this, and a security management still stricter than the 1st operation gestalt becomes possible.

[0043] (3rd operation gestalt) Drawing 4 is the block diagram of the microcomputer in which the 3rd operation gestalt of this invention is shown, and the common sign is given to the element in drawing 3 , and the common element.

[0044] This microcomputer has connected the same shift register 26 as drawing 1 to the initial value input side of this counter 29A while it is replaced with the counter 29 in drawing 3 and prepares counter 29A with an initializing function. Other configurations are the same as that of drawing 3 .

[0045] In such a microcomputer, discharge of the once set security bit is performed as follows.

[0046] First, debugging equipment is connected to the JTAG port 11, and a command with which a selector 22 chooses the 2nd input side is inputted. Thereby, the output side of counter 29A is connected to the address terminal of a flash ROM 18 through a selector 22. Moreover, the command which clears the value of a counter 30 to 0 is inputted.

[0047] Next, the n-th data DT 2 of the address AD 2 (here, it may be the n-th street) of arbitration and a flash ROM 18 are given to the JTAG port 11 from debugging equipment. The address AD 2 and data DT 2 are held through TAP24 at shift registers 26 and 25, respectively from the JTAG port 11.

[0048] Furthermore, the command for setting the content of maintenance of a shift register 26 as counter 29A as initial value is inputted from debugging equipment. By this, the value of counter 29A is set as n, reading appearance of the n-th content is carried out from a flash ROM 18, and it is given to

the 1st input side of a comparator 27 as data DT 1. On the other hand, the data DT 2 held at the shift register 25 are given to the 2nd input side of a comparator 27. Since data DT1 and DT2 are naturally equal, the output signal of a comparator 27 serves as "H", and the value of a counter 30 increases and is set to 1.

[0049] Then, while giving the n+1st data DT 2 of a flash ROM 18 to the JTAG port 11 from debugging equipment, only 1 makes the value of counter 29A increase by clock signal CK. Thereby, the data DT 2 given from debugging equipment are compared with the data DT 1 by which reading appearance was carried out from the n+1st street of a flash ROM 18. Since both are naturally equal, the value of a counter 30 increases and is set to 2. Subsequent actuation is the same as that of the 2nd operation gestalt.

[0050] As mentioned above, the microcomputer of this 3rd operation gestalt The shift register 25 holding the data DT 2 given to the JTAG port 11 through TAP24 by which direct continuation is carried out, and this TAP24, The shift register 26 holding the starting address for a comparison, and counter 29A which carries out sequential count-up of address signal AD2, and is given to a flash ROM 18, It has the counter 30 which compares the data DT 1 by which reading appearance was carried out from this flash ROM 18 with the data DT 2 given from debugging equipment, and counts the count of coincidence. Only those who know the stored data after the address of the arbitration of a flash ROM 18 are able to cancel a security bit by this, and a security management stricter than the 1st operation gestalt becomes possible. Moreover, since he is trying to check some stored data of a flash ROM 18, a security bit can be canceled rather than the 2nd operation gestalt in a short time.

[0051] (4th operation gestalt) Drawing 5 is the block diagram of the microcomputer in which the 4th operation gestalt of this invention is shown, and the common sign is given to the element in drawing 4 , and the common element.

[0052] This microcomputer was replaced with the flash ROM 18 in drawing 4 , and has formed the mask ROM (read-only memory which is not rewritable) 31. In connection with this, TAP14 and AND23 were deleted and the output side of an inverter 28 is connected to the control terminal of the switch section 12. Other configurations are the same as that of drawing 4 .

[0053] As for debugging of CPU16, in the case of the product which used such a mask ROM 31, it is always desirable from the relation of security that it is in a prohibition condition. however, the 1- the function which enables debugging of CPU16 from the problem of a test is required like the 3rd operation gestalt. It constitutes from this operation gestalt so that the function of TAP13 corresponding to CPU16 may be enabled based on the overflow signal OVF of a counter 30 like drawing 4 R> 4.

[0054] Therefore, the actuation for canceling a security function in this microcomputer is the same as that of the 3rd operation gestalt, and has the same advantage.

[0055] In addition, this invention is not limited to the above-mentioned operation gestalt, but various deformation is possible for it. As this modification, there is a thing as shown in the following (a) and (b), for example.

[0056] (a) The I/O signal of the JTAG port 11 is an example, and can be similarly applied to any interfaces.

[0057] (b) Logical level is arbitrary although positive logic explained the security signal SEQ and the control signal over the switch section 12.

[0058]

[Effect of the Invention] As explained to the detail above, when in agreement with the data with which the data inputted into the trial port were memorized by the store according to the 1st invention, the security discharge means which makes a switch an ON state is established. Thereby, even if the security bit is set, if the content of storage is known, CPU and storage can be accessed through a trial port.

[0059] According to the 2nd invention, the security discharge means has the address register and data

register which hold the address information inputted from the trial port, and data information, respectively. Furthermore, it has the comparator which compares the data by which reading appearance was carried out from the store based on address information with the data held at the data register. Thereby, security can be canceled only by inputting the data corresponding to the address and the address of arbitration.

[0060] According to the 3rd invention, the security discharge means has the data register holding the address counter which counts timing information and specifies a storage region, and the data information inputted from the trial port. Furthermore, when the count of coincidence of data reaches a predetermined value, it has the count counter of coincidence which outputs a discharge signal. Since a discharge signal is outputted by this in the phase whose contents of a fixed number of of storage corresponded, a stricter security management becomes possible.

[0061] According to the 4th invention, the security discharge means has the address register for setting up the initial value of an address counter according to the address information inputted from a trial port. Thereby, if the data after the address of arbitration are inputted and this data is in agreement, a discharge signal comes to be outputted and the time amount for security discharge can be shortened.

[0062] According to the 5th invention, when the data inputted into the trial port are compared with the data memorized by the store and both are in agreement, it has the security discharge means which makes a switch an ON state. Thereby, those who do not know the content of storage of storage cannot use a trial port, but can protect the security of CPU.

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## DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]

[Drawing 1] It is the block diagram of the microcomputer in which the 1st operation gestalt of this invention is shown.

[Drawing 2] It is the block diagram of the microcomputer which has the conventional security bit.

[Drawing 3] It is the block diagram of the microcomputer in which the 2nd operation gestalt of this invention is shown.

[Drawing 4] It is the block diagram of the microcomputer in which the 3rd operation gestalt of this invention is shown.

[Drawing 5] It is the block diagram of the microcomputer in which the 4th operation gestalt of this invention is shown.

[Description of Notations]

11 JTAG Port

12 Switch Section

13,14,24 TAP
16 CPU
18 Flash ROM
25 26 Shift register
27 Comparator
29, 29A, 30 Counter
31 Mask ROM

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